What is Claimed is:

1. A self-refresh apparatus comprising:

an internal address counter for outputting internal address in response to an internal operation signal;

a refresh controller for outputting the internal operation signal having a predetermined cycle in response to refresh command signals, and outputting a refresh operation signal having the predetermined cycle for selectively activating a bank when a partial bank refresh signal is applied for performing a partial array self-refresh on a bank; and

a row address strobe generator for selectively activating the bank in response to the refresh operation signal.

2. The apparatus according to claim 1, further comprising:

a command decoder for decoding a refresh command inputted externally, and for outputting the refresh command signal and a mode register set signal;

a refresh counter for outputting a signal having a predetermined cycle corresponding to a refresh rate in response to a self-refresh command signal out of the

refresh command signals;

a partial array self-refresh decoder for decoding and latching an extended mode register set code in response to the mode register set signal, and for selectively activating a plurality of control signals for performing a partial array self-refresh operation including the partial bank refresh signal by logically operating the latched code , in response to the self-refresh command signal; and

a row address pre-decoder for decoding the internal address into a row address and for outputting the row address.

3. The apparatus according to claim 1, wherein the refresh operation signal is selectively outputted in response to the partial bank refresh signal, and the internal operation signal is outputted in response to the signal having the predetermined cycle in a refresh mode regardless of the output of the refresh operation signal.

4. The apparatus according to claim 2, wherein a plurality of control signals outputted from the partial array self-refresh decoder include a first control signal for selectively activating the row address strobe generator in response to a partial array self-refresh type, and

second and third control signals for identifying the partial bank refresh signal.

5. The apparatus according to claim 4, wherein the refresh controller controls the refresh operation signal depending on states of the most significant bit of the internal address when the second control signal is activated.

6. The apparatus according to claim 4, wherein the refresh controller controls the refresh operation signal depending on states of the second most significant bit of the internal address when the third control signal is activated.

7. The apparatus according to claim 4, wherein the partial array self-refresh decoder decodes a 3 least significant bits of applied address and selectively outputs one of the first, second and third control signals.

8. The apparatus according to claim 4, wherein the row address strobe generator comprises:

a first row address strobe generator for selectively activating the bank in response to the refresh operation

signal in a refresh mode; and

a second row address strobe generator for selectively activating the other banks in response to the first control signal and the refresh operation signal in a refresh mode.

9. The apparatus according to claim 2, wherein the partial array self-refresh decoder comprises:

an extended mode register set decoder for decoding bank selecting address in response to the mode register set signal, and for outputting a register set control signal;

a plurality of address latches for decoding and latching the extended mode register set code in response to the register set control signal; and

a partial array self-refresh controller for selectively outputting one of the first, second and third control signals by logically operating the latched address.

10. A self-refresh method for performing a partial array self-refresh operation on a semiconductor memory,

wherein an internal address of the bank is continuously counted in a predetermined cycle corresponding to a refresh rate regardless of types of the partial array self-refresh when the partial array self-refresh operation is performed on a bank, and the bank is activated only when

the internal address is counted to a predetermined address depending on types of the partial array self-refresh.

11. A self-refresh method for performing a partial array self-refresh operation on a semiconductor memory in response to an extended mode register set code, comprising:

the first step of activating a refresh operation signal for activating a bank and an internal operation signal for counting internal address when a partial array self-refresh command on a bank is applied;

the second step of checking state change of a specific bit of the counted internal address depending on types of the partial array self-refresh; and

the third step of continuously activating the internal operation signal in a predetermined cycle regardless of state change of the specific bit, and of inactivating the refresh operation signal when the state of the specific bit is changed.

12. The method according to claim 11, wherein the second step checks state change of the most significant bit of the internal address when a self-refresh is performed on a half of a bank, and checks state change of the second most significant bit of the internal address when a self-

refresh is performed on a quarter of the bank.

13. The method according to claim 12, wherein the internal operation signal and the refresh operation signal are pulse signals having a predetermined cycle corresponding to a refresh rate.